REMARKS/ARGUMENTS

In the Office Action dated May 22, 2003, the Examiner: (1) objected to claims 7, 18 and 20 for informalities; (2) objected to claims 6-7, 13-14 and 16 as being dependent upon a rejected base claim; (3) rejected claims 1-3 and 8-10 as allegedly anticipated by *Krause* (U.S. Patent No. 5,914,953); and (4) rejected claims 4-5, 11-12, 15 and 17-21 as allegedly unpatentable over *Krause* in view of *Wasilewski* (U.S. Patent No. 5,457,701).

With this Preliminary Amendment, Applicants cancel claims 6-7, 13-14 and 16 in favor of those same claims in the parent case. Further, Applicants cancel claims 1, 2, 8 and 9, and amend claims 3, 4, 10, 11, 18 and 20. Applicants believe the pending claims are allowable over the art of record, and respectfully request reconsideration.

I. CLAIM OBJECTIONS

In the Office Action dated May 22, 2003 in the parent case, the Examiner objected to claims 7, 18 and 20 for various informalities. Claim 7 has been cancelled in favor of that same claim in the parent case. Claims 18 and 20 have been amended, as suggested by the Examiner.

II. CLAIM REJECTIONS

A. Claim 3

Claim 3 is directed to a computer system having a plurality of processors coupled together and between which messages may be routed. Each of the messages between the processors comprises a header tick and a data tick. Upon detecting an error has occurred, the processor alters the data tick error check bits in a predetermined manner. The Examiner rejected claim 3 as allegedly anticipated by *Krause*. Applicants amended claim 3 to be in independent form, including all the limitations of claim 1. Claim 3 already contained the limitations of claim 1 by virtue of its previous dependency from claim 1. Further, Applicants amended claim 3 to more clearly define that the alteration takes place in the error check bits.

"[F]or anticipation under 35 U.S.C. 102, the reference must teach every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present." MPEP § 706.02. *Krause* teaches that

a command symbol may be appended to each message indicating whether the message is good or bad.

> A command symbol -- "This packet[sic] Good" (TPG) or "This Packet Bad" (TPB) -- **is appended** to every packet.

Krause, Col. 5, lines 43-45 (emphasis added).

By contrast, claim 3 specifically requires that upon detecting an error, the processor alters the error check bits in a predetermined manner. *Krause* does not appear to teach or fairly suggest this feature of amended claim 3.

Based on the foregoing, Applicants respectfully submit that claim 3 should be allowed.

B. Claim 4

Claim 4 is directed to a computer system having a plurality of processors coupled together between which messages may be routed. Each of the messages between the processors comprises a header tick and a data tick. Upon detecting an error has occurred in the data tick, the processor replaces the bits of the data tick with a predetermined bit pattern. The Examiner rejected claim 4 as allegedly obvious over *Krause* in view of *Wasilewski*. The Applicants amended claim 4 to be in independent form, including all the limitations of claim 1. Claim 4 already contained the limitations of claim 1 by virtue of its previous dependency from claim 1. Further, Applicants amended the claim to more clearly indicate that when an error occurs, the bits of the data tick are replaced.

In rejecting claim 4, the Examiner states, "Krause does not specifically disclose replacing bits of information in the tick with a predetermined bit pattern." Office Action dated May 22, 2003, page 4. Applicants agree. The Examiner then relies upon *Wasilewski* for a teaching of "a pre-defined group of bits that are replaced with a second value when an uncorrectable error is detected." *Id.*

> [I]n accordance with the method of the present invention, a single bit in each packet, or alternatively, a group of bits, **is pre-defined as a 'packet error indicator[.]'**

Wasilewski, Col. 4, lines 19-23 (emphasis added).

> [A] one bit field 62 of each header 18 is pre-defined as a 'packet error indicator' ... . Whether a packet contains an uncorrectable bit

> error may be communicated through the value of the packet error indicator field 62.

Wasilewski, Col 5, lines 9-14; *Wasilewski* Figure 3. Thus, *Wasilewski* teaches a bit or group of bits in the header that are modified to indicate packet error.

Amended claim 4, by contrast, calls for replacing bits of the data tick. Applicants respectfully submit that the combination of *Krause* and *Wasilewski* does not teach or fairly suggest the limitations of amended claim 4. Further, *Wasilewski* teaches away from such a system.

> However, certain kinds of data, such as coded video data, may be useful despite an uncorrectable data error, and it would therefore be desirable to allow packets having uncorrectable data errors to continue through successive physical links to the ultimate reception site.

Wasilewski, Col. 1, lines 47-52. As defined by claim 4, at least some of the data is overwritten upon detection of an error.

Based on the foregoing, Applicants respectfully submit that claim 4, as well as claim 5 which depends from claim 4, should be allowed.

C. Claim 10

Claim 10 is directed to a processor that comprises a router capable of detecting transmission errors in a message. The message comprises a data block and a block comprising error check bits. Upon detecting that a transmission error has occurred in the message, the router alters the error check bits in a predetermined manner to indicate that the message contained the transmission error. The Examiner rejected claim 10 as allegedly anticipated by *Krause*. Applicants amended claim 10 to be in independent form, including all the limitations of claim 8. Claim 10 already contained the limitations of claim 8 by virtue of its previous dependency from claim 8. Further, Applicants amended claim 10 to more clearly indicate that a message comprises a data block and a block comprising error check bits, and that the router alters the error check bits to indicate that the message contains transmission errors.

Krause teaches appending a command symbol, being one of "This Packet Good" or "This Packet Bad," to every packet. *Krause*, Col. 5, lines 43-45. By contrast, claim 10 specifically requires the router alter the error check bits upon

detecting that a transmission error has occurred. Thus, *Krause* does not teach or fairly suggest altering error check bits upon detecting a transmission error.

Based on the foregoing, Applicants respectfully submit that claim 10 should be allowed.

D. Claim 11

Claim 11 is directed to a processor that comprises a router capable of detecting a transmission error in a message. The message comprises a data block and a header block. Upon detecting that a transmission error has occurred in the data block, the router replaces the bits of information in the data block with a predetermined bit pattern. The Examiner rejected claim 11 as allegedly obvious over *Krause* in view of *Wasilewski*. Applicants amended claim 11 to be in independent form, including all the limitations of claim 8. Claim 11 already contained the limitations of claim 8 by virtue of its previous dependency from claim 8. Further, Applicants amended claim 11 to more clearly indicate that a message comprises a data block and a header block, and that upon detecting a transmission error in the data block, the router replaces the bits of information in the data block. Applicants make this amendment to more clearly define over the teaching of *Wasilewski*.

In rejecting claim 4, the Examiner states, "Krause does not specifically disclose replacing bits of information in the tick with a predetermined bit pattern." Office Action dated May 22, 2003, page 4. Applicants agree. The Examiner relies upon *Wasilewski* for a teaching of "a pre-defined group of bits that are replaced with a second value when an uncorrectable error is detected." *Id.* However, the "pre-defined group of bits" in *Wasilewski* is a set of bits in a header, separate and apart from data bits and error bits. *See Wasilewski*, Col. 4, lines 19-23; Col. 5, lines 9-14; *Wasilewski* Figure 3.

Amended claim 11, by contrast, calls for replacing bits of the data. Since *Wasilewski* teaches only modifying bits in the header, Applicants respectfully submit that the combination of *Krause* and *Wasilewski* does not teach or fairly suggest the limitations of amended claim 11. Further, *Wasilewski* teaches away from a system that modifies the data. *See Wasilewski*, Col. 1, lines 47-52.

Based on the foregoing, Applicants respectfully submit that claim 11, and claim 12 which depends from claim 11, should be allowed.

E. Claim 15

Claim 15 is directed to a method of fault isolation in a multi-processor computer system that comprises, *inter alia*, replacing the erroneous portion of a message having an error with a predetermined bit pattern. The Examiner rejected claim 15 as allegedly obvious over *Krause* in view of *Wasilewski*.

The Examiner's primary reference, *Krause*, teaches that at each router crossing a command symbol, indicating that the packet is either good or bad, should be **appended** to every packet. *Krause*, Col. 5, lines 43-45. *Wasilewski* teaches that a bit field in a header is predefined as a "packet error indicator," and that this indicator field communicates whether the packet contains an uncorrectable bit error. *Wasilewski*, Col. 5, lines 9-14; *Wasilewski* Figure 3.

Claim 15, by contrast, specifically requires **replacing the erroneous portion of the message with a predetermined bit pattern**. Neither *Krause* nor *Wasilewski*, alone or in combination teach or fairly suggest the limitations of claim 15.

Based on the foregoing, Applicants respectfully submit that claim 15, and all claims which depend from claim 15 (claims 17-21), should be allowed.

III. CLAIM CANCELLATIONS

In addition to canceling claims 6-7, 13-14 and 16 in favor of those same claims in the parent case, Applicants have also cancelled claims 1, 2, 8 and 9. This cancellation is to narrow the issues before the Examiner, and is without prejudice to later asserting these claims, such as in a continuation application.

IV. CONCLUSION

Applicants respectfully request reconsideration and allowance of the pending claims. If the Examiner feels that a telephone conference would expedite the resolution of this case, he is respectfully requested to contact the undersigned.

In the course of the foregoing discussions, Applicants may have at times referred to claim limitations in shorthand fashion, or may have focused on a particular claim element. This discussion should not be interpreted to mean that

the other limitations can be ignored or dismissed. The claims must be viewed as a whole, and each limitation of the claims must be considered when determining the patentability of the claims. Moreover, it should be understood that there may be other distinctions between the claims and the prior art which have yet to be raised, but which may be raised in the future.

If any fees or time extensions are inadvertently omitted or if any fees have been overpaid, please appropriately charge or credit those fees to Hewlett-Packard Company Deposit Account Number 08-2025 and enter any time extension(s) necessary to prevent this case from being abandoned.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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